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EXAMINER
LEWIS, MONICA

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 02/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,417	FORBES, LEONARD	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to the amendment filed December 27, 2002.

Response to Amendment

2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Response to Arguments

3. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: a) 224 (See Figure 4); b) 242 (See Figure 5); c) OL1 and OL2 (See Figure 7A); and d) XG2 (See Figure 12). A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-15 and 18-22 are rejected under 35 U.S.C. 103(a) as obvious over Forbes et al. (U.S. Patent No. 5,936,274) in view of Kouznetsov et al. (U.S. Publication No. 2002/0142546).

In regards to claim 1, Forbes et al. ("Forbes") discloses the following:

a) a pillar (300) of semiconductor material that extends outwardly from a working surface of a substrate (305) to form a source region (310), a body region (320) and a drain region (315) of a floating gate transistor (See Figure 3A); and

b) a floating gate (325) along one side of the pillar (See Figure 3A).

In regards to claim 1, Forbes fails to disclose the following:

a) a control gate overlaying the floating gate.

However, Kouznetsov et al. ("Kouznetsov") discloses a semiconductor device that has a control gate overlaying a floating gate (See Figure 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Forbes to include a control gate overlaying a floating gate as disclosed in Kouznetsov because it aids in increasing memory density.

Additionally, since Forbes and Kouznetsov are both from the same field of endeavor, the purpose disclosed by Kouznetsov would have been recognized in the pertinent art of Forbes.

In regards to claim 2, Forbes discloses the following:

a) charges are selectively stored in the floating gate in programming the floating gate transistor (See Column 7 Lines 8-28).

In regards to claim 3, Forbes discloses the following:

a) the pillar is formed by etching (See Figure 7).

Additionally, the limitation of "pillar is formed by etching" makes it a product by process claim. The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claim 4, Forbes discloses the following:

a) an absence or a presence of stored charges on the floating gate determines a conductivity state of the transistor between the source region and the drain region (See Column 8 Lines 8-27).

In regards to claim 5, Forbes discloses the following:

a) the substrate is a bulk semiconductor substrate (See Column 1 Lines 47-49).

In regards to claim 6, Forbes discloses the following:

a) the substrate is a silicon on-insulator substrate (See Column 4 Lines 21 and 22).

In regards to claim 7, Forbes discloses the following:

a) hot electron injection is used to program the floating gate transistor (See Column 7 Lines 28-30).

In regards to claim 8, Forbes discloses the following:

a) Fowler-Nordheim tunneling is used to program the floating gate transistor (See Column 7 Lines 55-57).

In regards to claim 9, Forbes discloses the following:

a) a plurality of semiconductor stacks arranged in rows and in columns, wherein each stack forms source, body, and drain regions of a respective floating gate transistor (See Figure 3a);

b) a plurality of floating gates in trenches between the columns of semiconductor stacks, wherein the floating gates are separated from respective sides of the semiconductor stacks by a gate dielectric (340) (See Figure 3B); and

c) control gate (335) separated from the respective floating gates by an intergate dielectric (See Figure 4).

In regards to claim 9, Forbes fails to disclose the following:

a) a plurality of control gates overlaying the respective floating gates.

However, Kouznetsov discloses a semiconductor device that has a control gate overlaying a floating gate (See Figure 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Forbes to include a control gate overlaying a floating gate as disclosed in Kouznetsov because it aids in increasing memory density.

Additionally, since Forbes and Kouznetsov are both from the same field of endeavor, the purpose disclosed by Kouznetsov would have been recognized in the pertinent art of Forbes.

In regards to claim 10, Forbes discloses the following:

a) etching is used to form the plurality of semiconductor stacks which extend vertically from a substrate(See Figure 7).

Additionally, the limitation of "etching is used to form the plurality of semiconductor stacks" makes it a product by process claim. The MPEP § 2113, states, "Even though product - by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claim 11, Forbes discloses the following:

a) the respective floating gate transistors extend outwardly from a substrate with a source region formed proximally to the substrate, a body region above the source region, and a drain region above the body region (See Figure 3A).

In regards to claim 12, Forbes discloses the following:

a) two floating gates lie adjacent to each other in each trench between the columns of semiconductor stacks (See Figure 3A).

In regards to claim 12, Forbes fails to disclose the following:

a) one control gates overlays adjacent floating gates.

However, Kouznetsov discloses a semiconductor device that has a control gate overlaying a floating gate (See Figure 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Forbes to include a control gate overlaying a floating gate as disclosed in Kouznetsov because it aids in increasing memory density.

Additionally, since Forbes and Kouznetsov are both from the same field of endeavor, the purpose disclosed by Kouznetsov would have been recognized in the pertinent art of Forbes.

In regards to claim 13, Forbes fails to disclose the following:

a) one floating gate lie in each trench between the columns of semiconductor stacks, and one control gate overlays the floating gate (See Figure 3A and Figure 4).

In regards to claim 13, Forbes fails to disclose the following:

a) one control gates overlays adjacent floating gates.

However, Kouznetsov discloses a semiconductor device that has a control gate overlaying a floating gate (See Figure 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Forbes to include a control gate overlaying a floating gate as disclosed in Kouznetsov because it aids in increasing memory density.

Additionally, since Forbes and Kouznetsov are both from the same field of endeavor, the purpose disclosed by Kouznetsov would have been recognized in the pertinent art of Forbes.

In regards to claim 14, Forbes discloses the following:

a) two floating gates lie adjacent to each other in each trench between the columns of semiconductor stacks (See Figure 3A).

In regards to claim 14, Forbes fails to disclose the following:

a) two corresponding control gates lie adjacent to each other above the floating gates.

However, Kouznetsov discloses a semiconductor device that has a control gate overlaying a floating gate (See Figure 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Forbes to include a control gate overlaying a floating gate as disclosed in Kouznetsov because it aids in increasing memory density.

Additionally, since Forbes and Kouznetsov are both from the same field of endeavor, the purpose disclosed by Kouznetsov would have been recognized in the pertinent art of Forbes.

In regards to claim 15, Forbes discloses the following:

a) the array is a memory cell array with the source regions of common rows electrically connected to be first input selection lines the control gates electrically connected along the direction of the columns to be second input selection lines, and the drain regions of common columns electrically connected to output data lines (See Figure 1, Column 4 Lines 39-67, Column 5 Lines 1-25 and Column 6 Lines 25-65).

In regards to claim 18, Forbes discloses the following:

a) charges are stored in the floating gates to represent respective data in the memory cell array (See Column 7 Lines 8-28).

In regards to claim 19, Forbes discloses the following:

a) hot electron injection is used to selectively place charges in the respective floating gates, thereby programming the respective floating gate transistors (See Column 7 Lines 28-30).

In regards to claim 20, Forbes discloses the following:

a) a first conductivity type semiconductor pillar formed upon the substrate, wherein the pillar has top and side surfaces (See Column 1 Lines 64-67);

b) a first source/drain region of a second conductivity type formed in a portion of the pillar that is proximal to an interface between the pillar and the substrate (See Column 1 Line 67 and Column 2 Lines1 and 2);

c) a second source/drain region of a second conductivity type formed in a portion of the pillar that is distal to the substrate and separated from the first source/drain region (See Column 2 Lines 2-5);

d) a gate dielectric formed on at least a portion of one side surface of the pillar (See Figure 3B); and

e) a floating gate substantially adjacent to a portion of the side surface of the pillar and separated therefrom by the gate dielectric (See Figure 3B).

In regards to claim 20, Forbes fails to disclose the following:

a) an intergate dielectric formed on a top surface of the floating gate.

However, Kouznetsov discloses a semiconductor device that has an intergate dielectric formed on top of the floating gate (See Figure 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Forbes to include an intergate dielectric as disclosed in Kouznetsov because it aids in keeping the device from shortening out.

b) a control gate substantially overlaying the floating gate and insulated therefrom by the intergate dielectric.

However, Kouznetsov discloses a semiconductor device that has a control gate overlaying a floating gate separated by the intergate dielectric (See Figure 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Forbes to include a control gate overlaying a floating gate separated by the intergate dielectric as disclosed in Kouznetsov because it aids in increasing memory density.

Additionally, since Forbes and Kouznetsov are both from the same field of endeavor, the purpose disclosed by Kouznetsov would have been recognized in the pertinent art of Forbes.

In regards to claim 21, Forbes discloses the following:

a) electrical charges in the floating gate controls electrical conduction between the first source/drain region and the second source/drain region (See Column 5 Lines 8 and 9).

In regards to claim 22, Forbes discloses the following:

a) the floating gate transistor is a data storage element in a programmable memory array with the data represented by charges stored in the respective floating gates (See Column 7 Lines 13-16).

8. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as obvious over Forbes et al. (U.S. Patent No. 5,936,274) in view of Kouznetsov et al. (U.S. Publication No. 2002/0142546) and El Gamal et al. (U.S. Patent No. 5,510,730).

In regards to claim 16, Forbes discloses the following:

a) source regions of a common column electrically coupled to be selection lines, the control gates electrically coupled along the direction of the columns to be inputs, and the drain regions of a common row electrically coupled to be output lines (See Figure 1, Column 4 Lines 39-67, Column 5 Lines 1-25 and Column 6 Lines 25-65).

In regards to claim 16, Forbes fails to disclose the following:

a) logic array.

However, El Gamal et al. ("El Gamal") discloses a semiconductor device that has a logic array (See Column 2 Lines 5-13). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Forbes to include a logic array as disclosed in El Gamal because it aids in implementing logic functions.

Additionally, since Forbes and El Gamal are both from the same field of endeavor, the purpose disclosed by El Gamal would have been recognized in the pertinent art of Forbes.

In regards to claim 17, Forbes discloses the following:

a) source regions of a common column electrically interconnected, the drain regions of a common row electrically coupled to be output lines, and the control gates interconnected along the direction of the columns (See Figure 1, Figure 2, Figure 3, Column 4 Lines 39-67, Column 5 Lines 1-25 and Column 6 Lines 25-65).

In regards to claim 17, Forbes fails to disclose the following:

a) field programmable logic array.

However, El Gamal discloses a semiconductor device that has a field programmable logic array (See Figure 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Forbes to include a field programmable logic array as disclosed in El Gamal because it aids in implementing logic functions.

Additionally, since Forbes and El Gamal are both from the same field of endeavor, the purpose disclosed by El Gamal would have been recognized in the pertinent art of Forbes.

Conclusion

9. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Kumakura (European Publication No. 0498642A1) discloses a semiconductor memory device; b) Forbes et al. (U.S. Patent No. 6,104,061) discloses a memory cell with vertical transistors; c) Noble (U.S. Patent No. 5,973,352) discloses a high density flash memory; d) Burns, Jr. et al. (U.S. Patent No. 6,040,210) discloses a memory cell for memory applications; e) Shah (U.S. Patent No. 5,379, 255) discloses a three dimensional device; f) Burns, Jr. et al. (U.S. Patent No. 5,874,760) discloses a memory cell having vertical floating gate transistors; g) Noble et al. (U.S. Patent No. 6,486,027) discloses a field programmable logic array; h) Noble et al. (U.S. Publication No. 2002/0195649) discloses a field programmable logic array; h) Wong (U.S. Patent No. 5,386,132) discloses a multimedia storage system; i) Sugatani et al. (European Publication No. 0236676) discloses an erasable programmable read only memory; j) Hong (U.S. Patent No. 5,460,988) discloses a process high density flash EPROM cell; and k) Tamaki et al. (U.S. Patent No. 5,696,008) discloses a semiconductor device.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final

communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
January 17, 2003

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